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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04L 7/02

A1

(11) International Publication Number: WO 98/39873

(43) International Publication Date: 11 September 1998 (11.09.98)

(21) International Application Number: PCT/US98/04179

(22) International Filing Date: 4 March 1998 (04.03.98)

(30) Priority Data:

60/039,802	4 March 1997 (04.03.97)	US
09/033,769	3 March 1998 (03.03.98)	US

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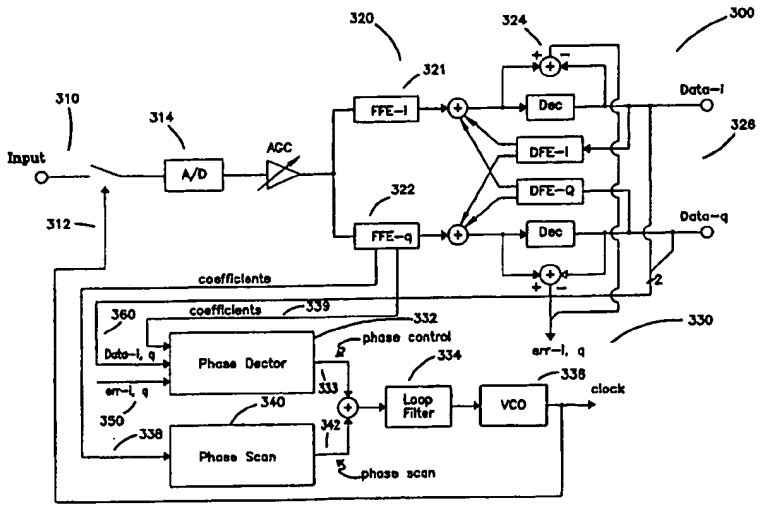
(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published

With international search report.

(54) Title: APPARATUS AND METHOD FOR PERFORMING TIMING RECOVERY



(57) Abstract

A timing recovery circuit is disclosed that prevents phase error over–compensation. The timing recovery circuit includes a phase scanner for determining when phase error over–compensation has occurred and generating a signal for preventing dual phase compensation in response thereto, thereby providing an accurate recovered clock signal. The timing recovery circuit also includes a feed–forward equalizer having a plurality of taps providing coefficients for filtering and adapting the input timing recovery circuit to an input signal. The phase scanner compares the tap coefficients to generate signal for preventing phase over–compensation by the feed–forward equalizer. A phase detector is provided for sampling coefficients from the feed–forward equalizer, error signals and output data and generating a phase signal used to generating the recovered clock signal. The signal for preventing phase over–compensation is mixed with the phase signal to generate the recovered clock signal.

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APPARATUS AND METHOD FOR PERFORMING TIMING RECOVERY

BACKGROUND OF THE INVENTION

Field of the Invention.

This invention relates in general to a timing recovery system and method, and more particularly to a phase-locked loop timing recovery system and method which is highly effective in eliminating re-activation.

Description of Related Art.

At a receiver in a typical communication system, an analog-to-digital converter is utilized to convert a received continuous-time signal into a discrete-time format. One problem which is encountered in this type of system is that the local receiver clock and the remote transmitter clock are asynchronous. If the receiver clock is slower than the transmitter clock, after a long enough period of time, one sample of the received continuous-time signal will be lost. On the other hand, if the local receiver clock is faster than the remote transmitter clock, after a long enough period of time, an extra sample of the received continuous-time signal will be obtained. Thus, the problem of recovering the clock signal is an important problem in many communication systems.

Recently, several high speed digital data services have become commercially available. These high speed digital data services are known as the ISDN(Integral Services Digital Network) basic rate, HDSL(High Speed Digital Subscriber Loop), HDSL2(High Speed Digital Subscriber Loop 2), ADSL(Asymmetric Digital Subscriber Loop), and Tl services.

In these transmission system, the transceiver needs to recover the clock signal to provide the high speed services. In particular, a phase-locked loop (PLL) is need to obtain the clock signal. At the slave side(normally called Remote side, RT), the loop timing needed to be acquired from the received signal sent from the master side(normally called Central Office side, CO). The RT transmitter sends back a signal to the CO side with the synchronous time base acquired in its receiver phase-locked loop. Further, some systems use the signal carrierless AM/PM (CAP) or quadrature amplitude modulation (QAM) signal as the line code, which is very effective when the cable loss is heavily distorted due to skin effect of the cable and the open-ended stub, bridged taps.

One prior phase-locked loop method 100 is illustrated in Fig. 1. In Fig. 1, an input signal 110 is sampled according to a clock signal 112 and input to an analog-to-digital converter 114. The digital output of the analog-to-digital converter 114 is passed

through the feed-forward equalizer 120 and the decision feedback equalizer 122 to produce the output data 124. To recover the clock signal 112, the input is sampled and rectified by the rectifier 130. Then the rectified signal is passed through a high Q bandpass filter 140. The output of the bandpass filter 140 is then passed to a comparator 150 for determining the clock signal based upon, for example, a comparison of the output of the bandpass filter and a threshold signal.

The phase-locked loop circuit 100 in Fig. 1 needs a high-Q bandpass filter 140 to extract the carrier component of the input signal 110. However, this method is not practical to implement with CMOS circuitry, since highly accurate LC components 160 that are needed to achieve the high Q bandpass filter 140 can not be accurately controlled by the current CMOS technology. Hence, such a system 100 needs expensive external components.

Yet another prior method 200 is illustrated in Fig. 2. The phase-locked loop circuit 200 illustrated in Fig. 2 shows the sampling of an input signal 210 according to a derived clock signal 212, which is then provided to an analog-to-digital converter 214. The digital output of the analog-to-digital converter is passed through the fractionally spaced feed-forward equalizer 220 and the decision feedback equalizer 224 to produce the output data.

The output of the fractionally spaced feed-forward equalizer 220 provides an input to the phase-locked loop 230. From the output of the fractionally spaced feed-forward equalizer 224, the phase is determined by a phase detector 232 which is then passed through a loop filter 234. The loop filter 234 controls a voltage-controlled oscillator 236 to generate the clock signal 212.

However, the fractionally spaced feed-forward equalizer 220 tends to adjust phase error by itself, i.e., the fractionally spaced feed-forward equalizer 220 only needs the frequency adjustment. However, the phase-locked loop 230 also tries to detect and adjust for phase error. Therefore, this dual phase error compensation via the two paths fight each other and do not converge. Thus, this method requires re-acquisition because of the meta-stability caused by the mutual interaction between phase-locked loop 230 and the feed-forward equalizer 224.

Regarding this meta-stability, the feed-forward equalizer 224 has to be a fractionally spaced feed forward equalizer (FFE) to achieve high transmission quality of the bit error rate performance under the hash cable environment described above. The fractional spaced feed forward equalizer is basically finite impulse response (FIR) filter. Since, the FIR filter is fractionally spaced, i.e., the input is sampled N times faster than the symbol speed and fed to the FIR which has the unit delay of Tsymbol/N, where

Tsymbol is the symbol period, the timing is self-adjusted. Therefore, it is not easy to extract correct timing information from the equalizer parameters.

It can been seen, then, that there is a need for an effective technique to acquire timing in digital data network.

It can be seen that there is a need for a phase-locked loop and method that is implemented using current CMOS circuit technology and which is highly effective in eliminating re-activation.

SUMMARY OF THE INVENTION

To overcome the limitations in the prior art described above, and to overcome other limitations that will become apparent upon reading and understanding the present specification, the present invention discloses a phase-locked loop timing recovery system and method which is highly effective in eliminating re-activation.

The present invention solves the above-described problems by providing a timing recovery circuit that prevents phase error over-compensation.

A system in accordance with the principles of the present invention includes a phase scanner for determining when phase error over-compensation has occurred and generating a signal for preventing dual phase compensation in response thereto thereby providing an accurate recovered clock signal.

Other embodiments of a system in accordance with the principles of the invention may include alternative or optional additional aspects. One such aspect of the present invention is that the timing recovery circuit includes a feed-forward equalizer having a plurality of taps providing coefficients for filtering and adapting the input timing recovery circuit to an input signal.

Another aspect of the present invention is that the phase scanner compares the tap coefficients to generate signal for preventing phase over-compensation by the feed-forward equalizer.

Another aspect of the present invention is that the timing recovery circuit further includes a phase detector for sampling coefficients from the feed-forward equalizer, error signals and output data and generating a phase signal used to generating the recovered clock signal.

Another aspect of the present invention is that the signal for preventing phase over-compensation is mixed with the phase signal to generate the recovered clock signal.

Yet another aspect of the present invention is that the feed-forward equalizer is a fractionally spaced feed-forward equalizer.

Another aspect of the present invention is that the phase scanner further includes a comparator for comparing two taps from the feed-forward equalizer to generate a comparator output signal indicating whether over-compensation by the feed-forward equalizer has occurred, the comparator output signal being mixed with a scan phase signal to generate the signal for preventing phase over-compensation by the feed-forward equalizer.

Another aspect of the present invention is that the phase detector further includes a first circuit for processing a center tap from the feed-forward equalizer and a reference signal to generate a first control signal and a second circuit for processing the error signals and the data output signal to generate a second control signal, the first and second control signal being combined to produce the phase control signal.

Still another aspect of the present invention is that the second circuit further includes a first mixer for combining a first error signal and a first data signal to produce a first product signal and a second mixer for combining a second error signal and a second data signal to produce a second product signal, the first and second product signal being combined and integrated by a predetermined factor to produce the second control signal.

Another aspect of the present invention is that the digital signal is split into a in-phase and quadrature signal, and the feed-forward equalizer further includes an in-phase feed-forward equalizer for processing the in-phase signal and a quadrature feed-forward equalizer for processing the quadrature signal, and wherein the first error signal is an in-phase error signal and the second error signal is a quadrature error signal and the first data signal is an in-phase data signal and the second data signal is a quadrature data signal.

These and various other advantages and features of novelty which characterize the invention are pointed out with particularity in the claims annexed hereto and form a part hereof. However, for a better understanding of the invention, its advantages, and the objects obtained by its use, reference should be made to the drawings which form a further part hereof, and to accompanying descriptive matter, in which there are illustrated and described specific examples of an apparatus in accordance with the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

Fig. 1 illustrates a first prior phase-locked loop method;

Fig. 2 illustrates a second prior phase-locked loop method;

Fig. 3 illustrates a block diagram of the timing recovery system according to the present invention;

Figs. 4a and 4b illustrated the detail block diagrams for the main phase detector and the phase scan respectively;

Fig. 5 shows that CAP isolated pulses for I and Q pulses;

Fig. 6 illustrates the waveforms for the outputs of FFE-i and FFE-q of Fig 3; and

Fig. 7 illustrates a detailed circuit diagram of a timing recovery circuit according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following description of the exemplary embodiment, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration the specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized as structural changes may be made without departing from the scope of the present invention.

The present invention provides a phase-locked loop and method that is implemented using current CMOS circuit technology and which is highly effective in eliminating re-activation. Particularly, the phase-locked loop system and method is effective for a system which uses carrierless AM/PM (CAP) or quadrature amplitude modulation (QAM) line code.

Fig. 3 illustrates a block diagram of the timing recovery system 300 according to the present invention. The timing recovery system 300 samples an input signal 310 according to a derived clock signal 312. The sampled input signal 310 is then provided to an analog-to-digital converter 314. The digital output of the analog-to-digital converter 314 is passed through to a feed-forward equalizer 320 and a decision feedback equalizer 324 to produce the output data 326. The feed forward equalizer 320 adapts to the line response so that the node immediately prior to the decision feedback equalizer (DFE) 324 sees no precursor intersymbol interference (ISI) which cannot be cancelled.

The output of the feed-forward equalizer 320 also provides an input to a phase-locked loop 330. The output of the feed-forward equalizer 320 is provided to a phase detector 332 for generating a phase control signal 333 that is provided to a loop filter 334. The loop filter 334 controls a voltage-controlled oscillator 336 to generate the clock signal. However, in the timing recovery circuit 300 of Fig. 3, coefficients 338 from the feed-forward equalizer 320 are passed to a phase scanner 340 that provides a phase

scan signal 342 which is combined with the phase control signal 333 from the phase detector 332.

The main phase detector 332 creates the useful timing information from the several tap coefficient values 339 in the feed-forward equalizer 320, error signals 350, and recovered data 360. The frequency scan block 340 monitors the relation between feed-forward equalizer coefficient values 338 and when it judges that the coefficient values 338 are in the wrong state, the frequency scanner 340 forces the phase-locked loop 330 to create a phase jump to eliminate the phase-locked loop from being stuck at the wrong stable phase.

Two control signals 333, 342 from the main phase detector 332 and phase scanner 340 respectively are added together and fed to the loop filter 334 to drive the voltage control oscillator. The controlled clock signal 312 then is used to determine the sampling instance of the input signal 310 which is quantized by the A/D converter 314.

Figs. 4a and 4b illustrated the detail block diagrams for the main phase detector 410 and the phase scan 450 respectively. In Fig. 4a, by way of example, only one feed-forward equalizer coefficient 412, H(n1), is used in the phase detector. The reference value 414, REF, is subtracted from coefficient H(n1) 412 which is then multiplied by the amplifier 416 by a gain factor 418, G. This process creates one of the two control signals, control-1 420.

On the other hand, the two products 422, 424 are calculated from the combination of err-i 426, err-q 428, data-i 430, and data-q 432. The two products 422, 424 are added 434 and integrated 436 by a factor, Z to generate the second control signal, control-2 440. The second control signal, control-2 440, is added with control-1 to form the final phase control signal 442 at the output of phase detector.

Fig. 4b illustrates an detailed embodiment for the phase scanner 450. In Fig. 4b, two coefficients 452, 454 are compared in comparator 460. The output 462 of the comparator 460 is a logic one if the first coefficient 452 to the comparator 460 is greater than the second coefficient 454 to the comparator 460. The output 462 of the comparator 460 is a logic zero if the first coefficient 452 to the comparator 460 is less than or equal to the second coefficient 454 to the comparator 460. The output 462 of the comparator 460 is mixed with the scan phase 470 to generate the phase scan control signal 472.

Fig. 5 shows that CAP isolated pulses for I 510 and Q 520 pulses. These pulses 510, 520 are fed to the two parallel feed-forward equalizers, FFE-i 321 and FFE-q 322, respectively as shown in Fig. 3.

The waveforms 600 shown in Fig. 6 are the outputs of FFE-i 321 and FFE-q 322 of Fig. 3 for those CAP isolated pulses. For example, for the case for the null cable

and after feed-forward equalizers are converged, CAP I and Q isolated pulses are fed to the input at different times and plotted on the same time axis. As can be seen in this figure, plot A 620 and C 624 are the output of FFE-i 321 and FFE-q 322 when I pulse is sent and plot B 622 and D 626 are FFE-q 321 and FFE-i 322 outputs driven by the CAP Q pulse. Fig. 6 demonstrates that the timing information is created by the combination of products as shown below in equation 1.

$$\text{Timing Information} = \text{err-q*out-i} - \text{err-i*out-q} \quad \text{Eqn. 1}$$

Fig. 7 illustrates a detailed circuit diagram of a timing recovery circuit 700 according to the present invention. In Fig. 7, the center tap of the FFE-q 722 is used for the H(n1) 770 previously described in Fig. 4a and Reference is set to zero. The gain 772, G, is set to 5.0. The comparison of +/-2 tap positions 774, 776 of FFE-q 721 is used to drive the Phase Scanner 740 as described in Fig. 4b. The control of AGC is performed according to equation 2:

$$\text{AGC=AGC-(err-i*out-i + err-q*out-q)/2**mue} \quad \text{Eqn. 2}$$

where AGC is the AGC gain and mue is the typically select to be in a range between 14 and 20.

As shown in Fig. 7, the scan path 740 is used to eliminate the problem of dual phase error compensations. The scan path forces the feed-forward equalizer 720 not to make a phase compensation. This can be done by monitoring the two feed-forward equalizer FFE-q 722 coefficient values: (H(n3)) 776 and (H(n2)) 774. This can be explained by looking at Fig. 5.

If the best timing phase is assumed to be the top of the I-signal, around t=8.2 530, from the nature of the CAP signal, in this example, the Q-signal has zero-crossing 540 at around this optimal timing phase. When the feed-forward equalizer tries to compensate the phase error from this optimal timing, feed-forward equalizer coefficients shown in Fig. 7, H(n2) 774 and H(n3) 776 will change their values. For example, when the phase is delayed, the H(n2) 774 value becomes bigger and H(n3) 776 becomes smaller. The scan control 740 uses these characteristics and when it detects that the feed-forward equalizer FFE-q 722 has over-compensated for the phase error, the scan control 740 sends an output 742 which is added to phase control signals control-1 780 and control-2 782. Thus, the scan control eliminates dual phase error compensation.

The foregoing description of the exemplary embodiment of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not with this detailed description, but rather by the claims appended hereto.

WHAT IS CLAIMED IS:

1. A timing recovery circuit comprising a phase scanner for determining when phase error over-compensation has occurred and generating a signal for preventing dual phase compensation in response thereto thereby providing an accurate recovered clock signal.

2. The timing recovery circuit of claim 1 further comprising a feed-forward equalizer having a plurality of taps providing coefficients for filtering and adapting the input timing recovery circuit to an input signal.

3. The timing recovery circuit of claim 2 wherein the phase scanner compares the tap coefficients to generate signal for preventing phase over-compensation by the feed-forward equalizer.

4. The timing recovery circuit of claim 3 further comprising a phase detector for sampling coefficients from the feed-forward equalizer, error signals and output data and generating a phase signal used to generating the recovered clock signal.

5. The timing recovery circuit of claim 4 wherein the signal for preventing phase over-compensation is mixed with the phase signal to generate the recovered clock signal.

6. The timing recovery circuit of claim 2 wherein the feed-forward equalizer is a fractionally spaced feed-forward equalizer.

7. The timing recovery circuit of claim 2 wherein the phase scanner further comprising a comparator for comparing two taps from the feed-forward equalizer to generate a comparator output signal indicating whether over-compensation by the feed-forward equalizer has occurred, the comparator output signal being mixed with a scan phase signal to generate the signal for preventing phase over-compensation by the feed-forward equalizer.

8. The timing recovery circuit of claim 7 wherein the phase detector further comprises a first circuit for processing a center tap from the feed-forward equalizer and a reference signal to generate a first control signal and a second circuit for processing the

error signals and the data output signal to generate a second control signal, the first and second control signal being combined to produce the phase control signal.

9. The timing recovery circuit of claim 8 wherein the second circuit further comprises a first mixer for combining a first error signal and a first data signal to produce a first product signal and a second mixer for combining a second error signal and a second data signal to produce a second product signal, the first and second product signal being combined and integrated by a predetermined factor to produce the second control signal.

10. The timing recovery circuit of claim 9 wherein the digital signal is split into a in-phase and quadrature signal, and the feed-forward equalizer further comprising an in-phase feed-forward equalizer for processing the in-phase signal and a quadrature feed-forward equalizer for processing the quadrature signal, and wherein the first error signal is an in-phase error signal and the second error signal is a quadrature error signal and the first data signal is an in-phase data signal and the second data signal is a quadrature data signal.

11. A timing recovery circuit, comprising:

a switch for sampling an incoming line code signal, the switch sampling the incoming signal according to a recovered clock signal;

a analog-to-digital converter, coupled to the switch, for converting the incoming line code signal to a digital signal;

a feed forward equalizing means, coupled to the analog-to-digital converter, for receiving the digital signal and for filtering the incoming signal, wherein the feed-forward equalizer includes a plurality of taps and the feed-forward equalizer filtering the input signal to adapted the input signal to the line code;

a decision feedback equalizer, coupled to the feed forward equalizer, for cancelling intersymbol interference in the filtered signal and generating error signals and a data output signal; and

a phase-locked loop, coupled to the feed forward equalizer, for generating the recovered clock signal in response to a signal received from the feed forward equalizer, the phase-locked loop further comprising:

a phase detector for generating a phase signal based upon tap coefficients from the feed forward equalizer, and error signals and a data output from the decision feedback equalizer; and

a phase scanner, coupled to the feed-forward equalizer, for determining when phase error over-compensation has occurred and generating a signal for preventing dual phase compensation in response thereto, the phase signal and the signal for preventing dual phase compensation being combined to derive a recovered clock signal.

12. The timing recovery circuit of claim 7 wherein the phase-locked loop further comprises a loop filter and a voltage controlled oscillator, the combination of the phase signal and the signal for preventing dual phase compensation driving the loop filter and voltage controlled oscillator to generate the recovered clock signal.

13. The timing recovery circuit of claim 11 wherein the feed-forward equalizer is a fractionally spaced feed-forward equalizer.

14. The timing recovery circuit of claim 11 wherein the phase scanner further comprising a comparator for comparing two taps from the feed-forward equalizer to generate a comparator output signal indicating whether over-compensation by the feed-forward equalizer has occurred, the comparator output signal being mixed with a scan phase signal to generate the signal for preventing phase over-compensation by the feed-forward equalizer.

15. The timing recovery circuit of claim 14 wherein the phase detector further comprises a first circuit for processing a center tap from the feed-forward equalizer and a reference signal to generate a first control signal and a second circuit for processing the error signals and the data output signal to generate a second control signal, the first and second control signal being combined to produce the phase control signal.

16. The timing recovery circuit of claim 15 wherein the second circuit further comprises a first mixer for combining a first error signal and a first data signal to produce a first product signal and a second mixer for combining a second error signal and a second data signal to produce a second product signal, the first and second product signal being combined and integrated by a predetermined factor to produce the second control signal.

17. The timing recovery circuit of claim 16 wherein the digital signal is split into a in-phase and quadrature signal, and the feed-forward equalizer further comprising an in-phase feed-forward equalizer for processing the in-phase signal and a quadrature feed-forward equalizer for processing the quadrature signal, and wherein the first error

signal is an in-phase error signal and the second error signal is a quadrature error signal and the first data signal is an in-phase data signal and the second data signal is a quadrature data signal.

18. A method for recovering a clock signal from a input signal, comprising the steps of:

receiving an input signal;

filtering the input signal to generate a data signal,

sampling the filtered input signal to determine when phase error over-compensation has occurred;

generating a signal for preventing dual phase compensation in response to a determination that the filtered input signal has been phase error over-compensated; and

processing the signal for preventing dual phase compensation to provide a recovered clock signal.

19. The method of claim 18 wherein the step of filtering the input signal further comprises the step of generating a plurality of taps providing tap coefficients.

20. The method of claim 19 wherein the step of sampling the filtered input signal to determine when phase error over-compensation has occurred further comprises the steps of sampling coefficients and generating a phase scan signal for preventing error over-compensation, the phase scan signal being used to generate the recovered clock signal.

21. The method of claim 20 wherein the step of processing the signal for preventing dual phase compensation further comprises the step of mixing the signal for preventing phase over-compensation with a phase signal to generate the recovered clock signal.

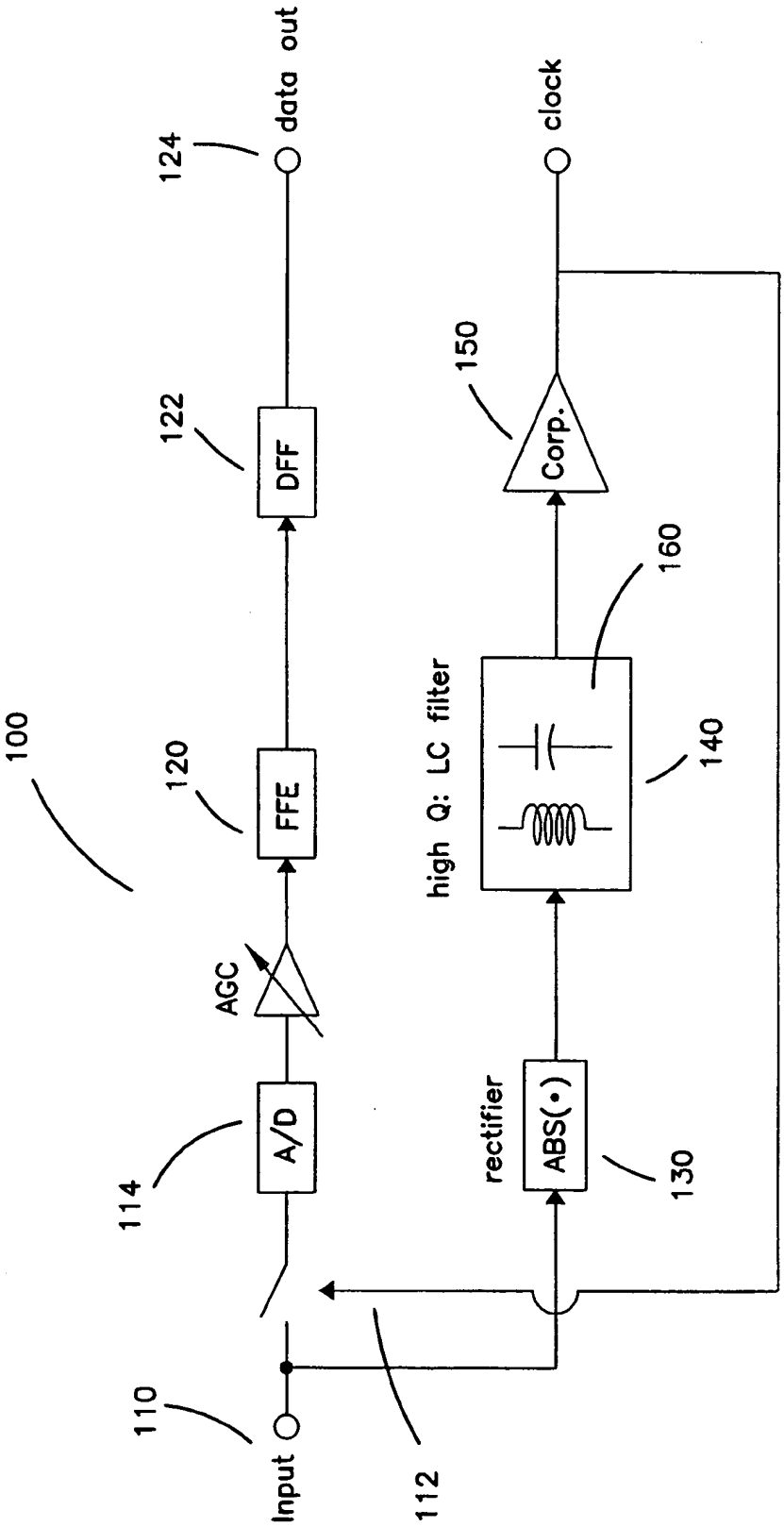

FIG. 1
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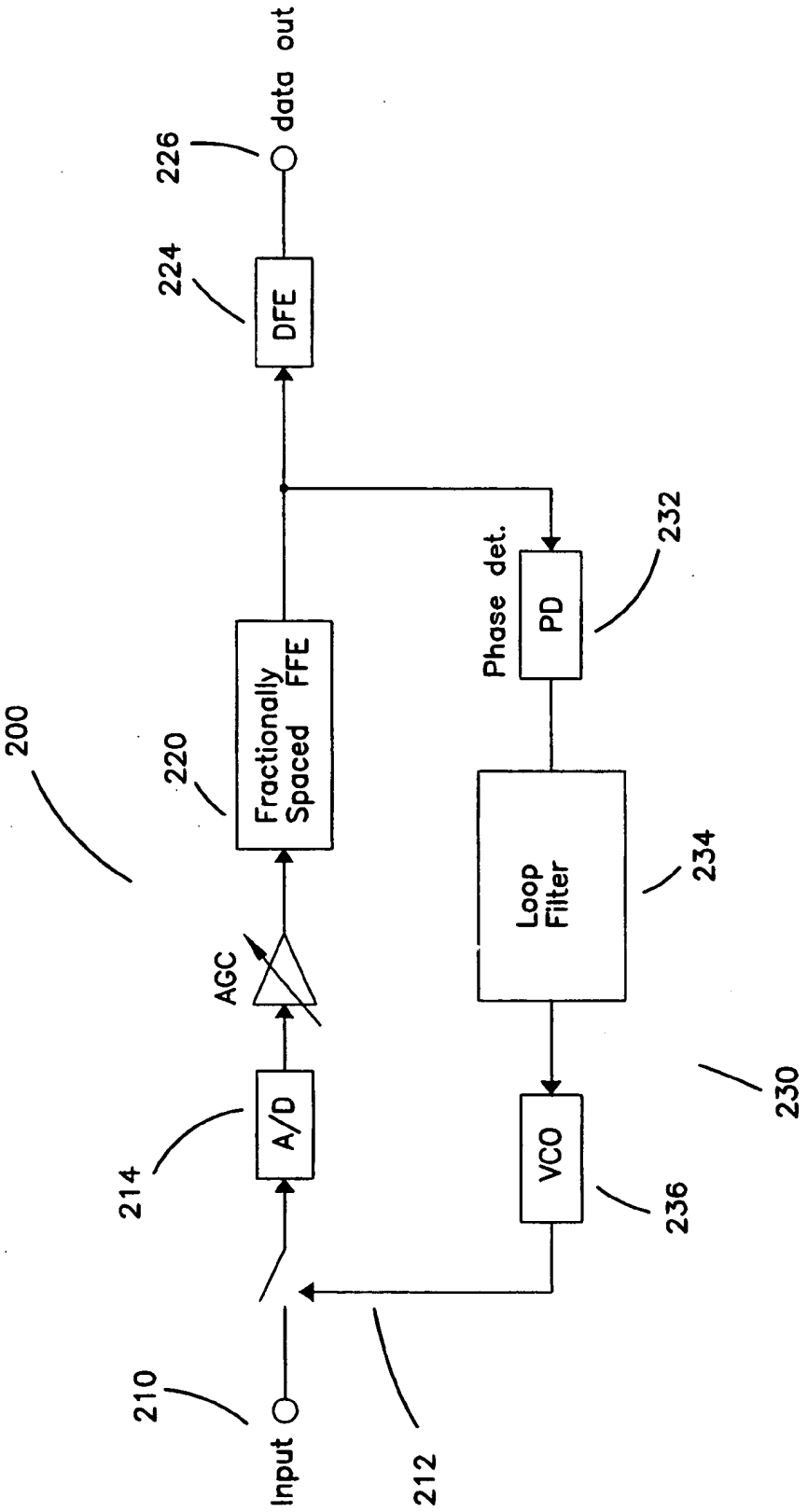

FIG. 2
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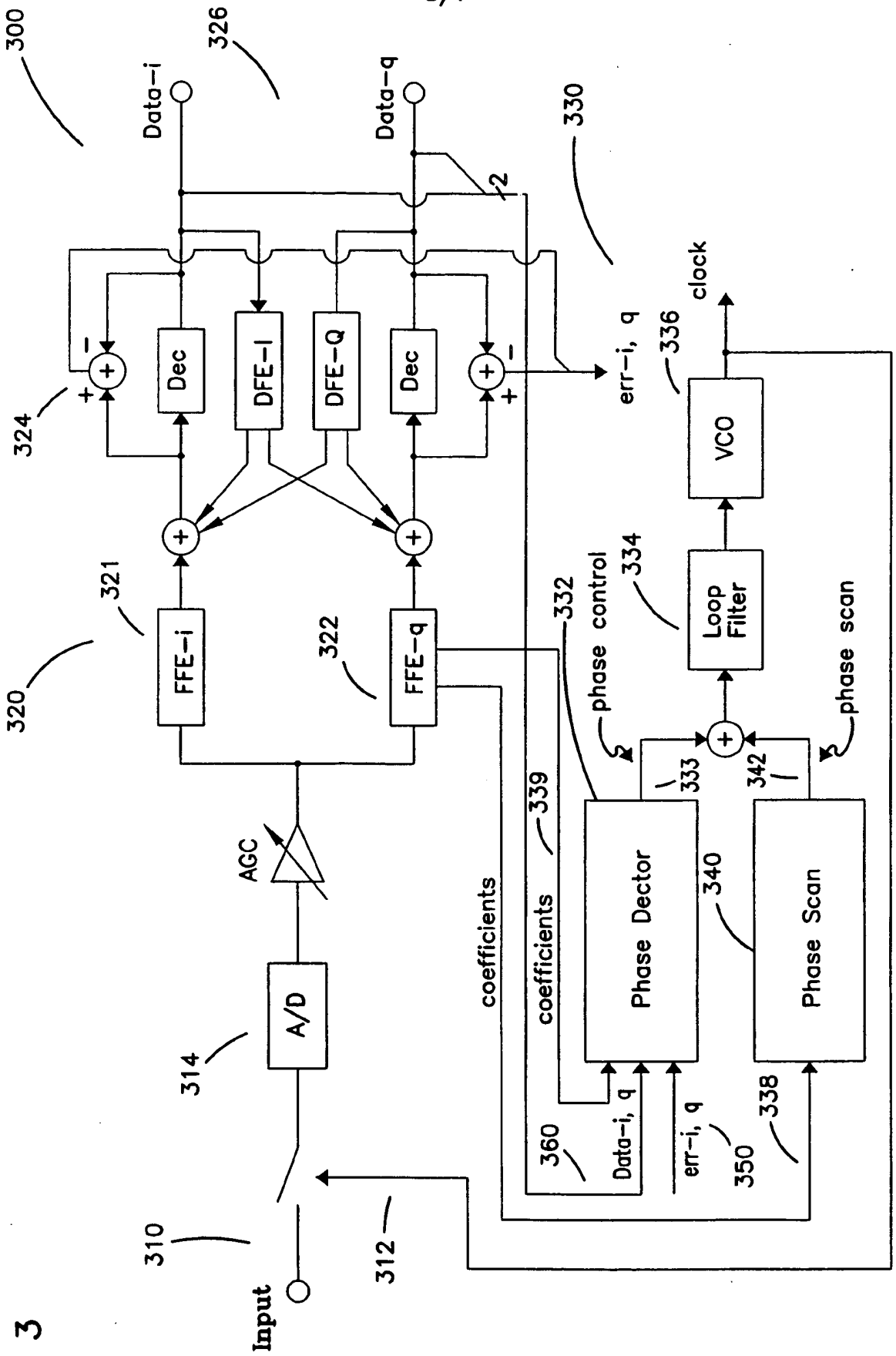
300
326
Data-i
Data-q
330
12
clock
336
VCO
Loop Filter
334
phase control
phase scan
332
339
coefficients
coefficients
Phase Dector
340
Phase Scan
338
360
Data-i, q
err-i, q
350
333
342
324
Dec
DFE-I
DFE-Q
Dec
err-i, q
321
322
320
FFE-i
FFE-q
AGC
A/D
314
310
312
Input

FIG. 3

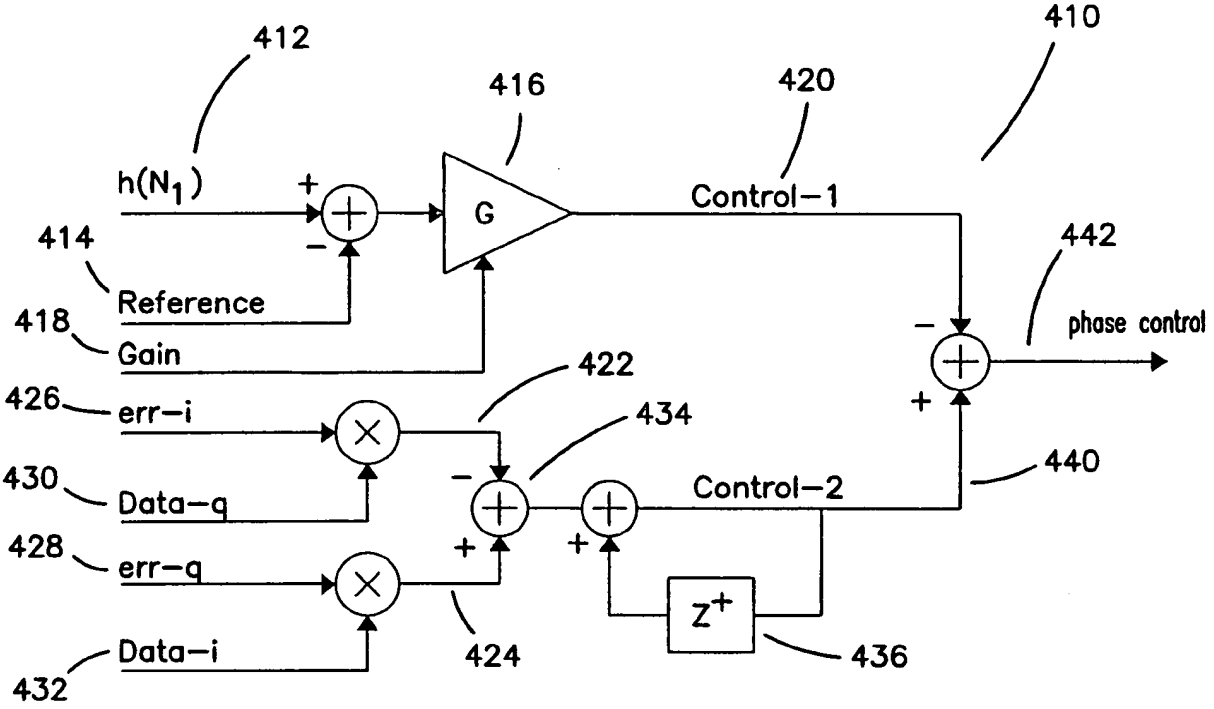
412
410
416
420
h(N1)
+
G
Control–1
414
Reference
442
418
Gain
phase control
422
426
err–i
434
430
Data–q
Control–2
440
428
err–q
+
+
Z+
424
436
Data–i
432

FIG. 4A

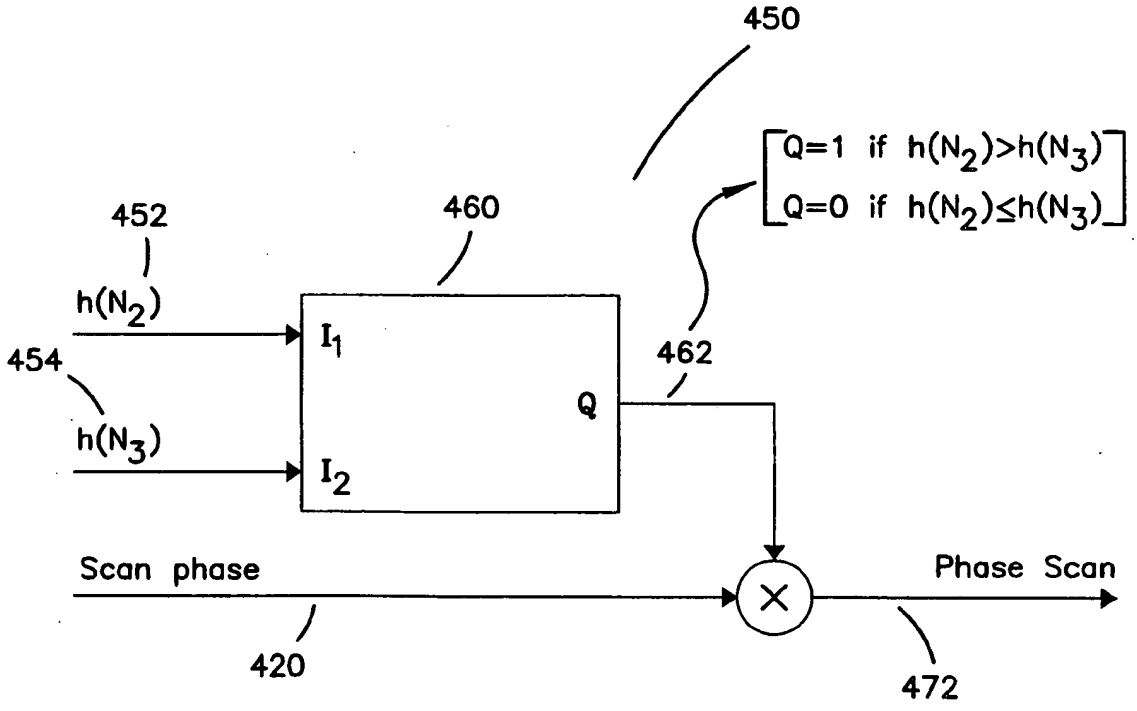
450
Q=1 if h(N2)>h(N3)
Q=0 if h(N2)≤h(N3)
452
460
h(N2)
I1
462
454
Q
h(N3)
I2
Scan phase
Phase Scan
420
472

FIG. 4B

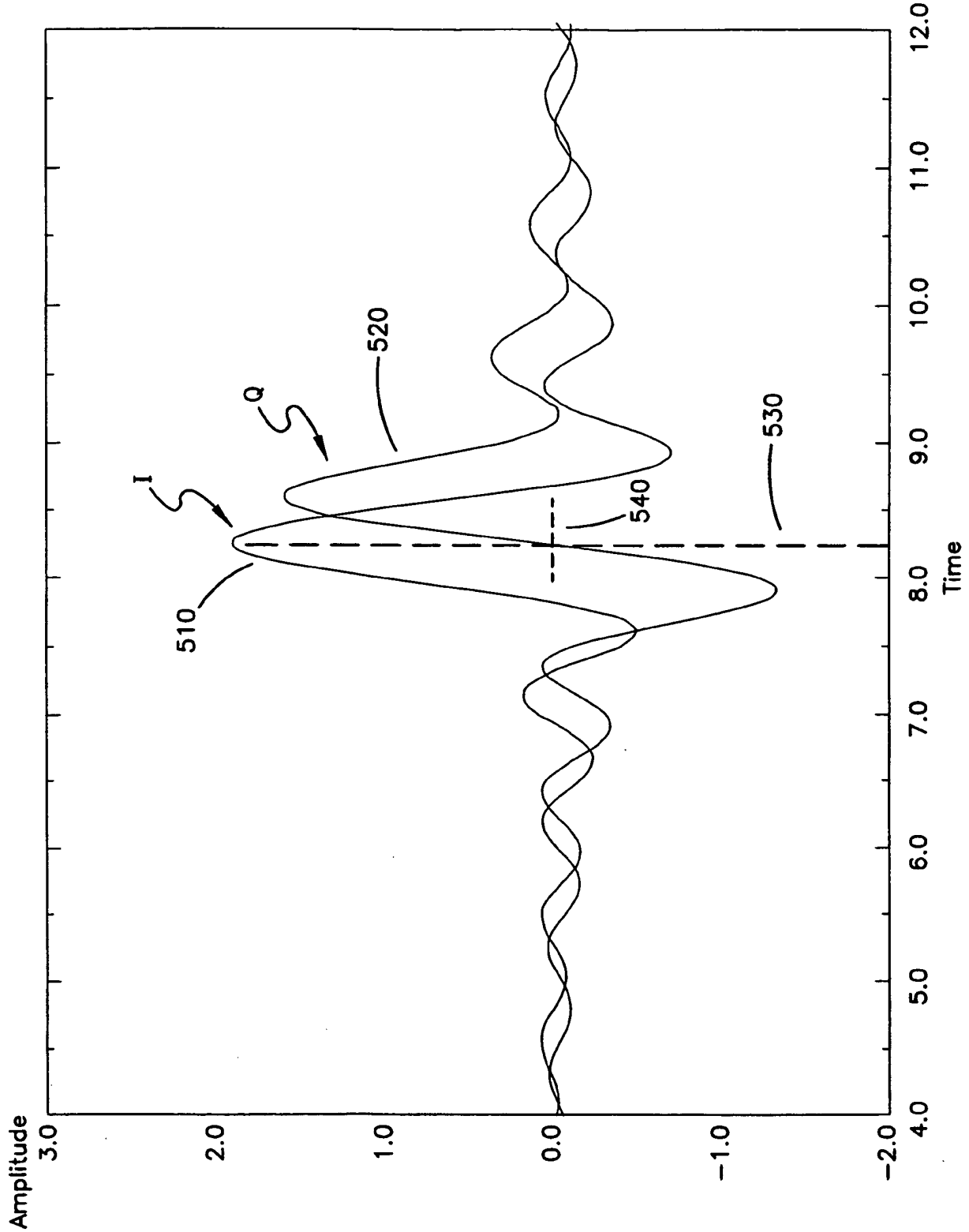
Amplitude
3.0
2.0
1.0
0.0
−1.0
−2.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
11.0
12.0
Time
I
Q
510
520
530
540

FIG. 5

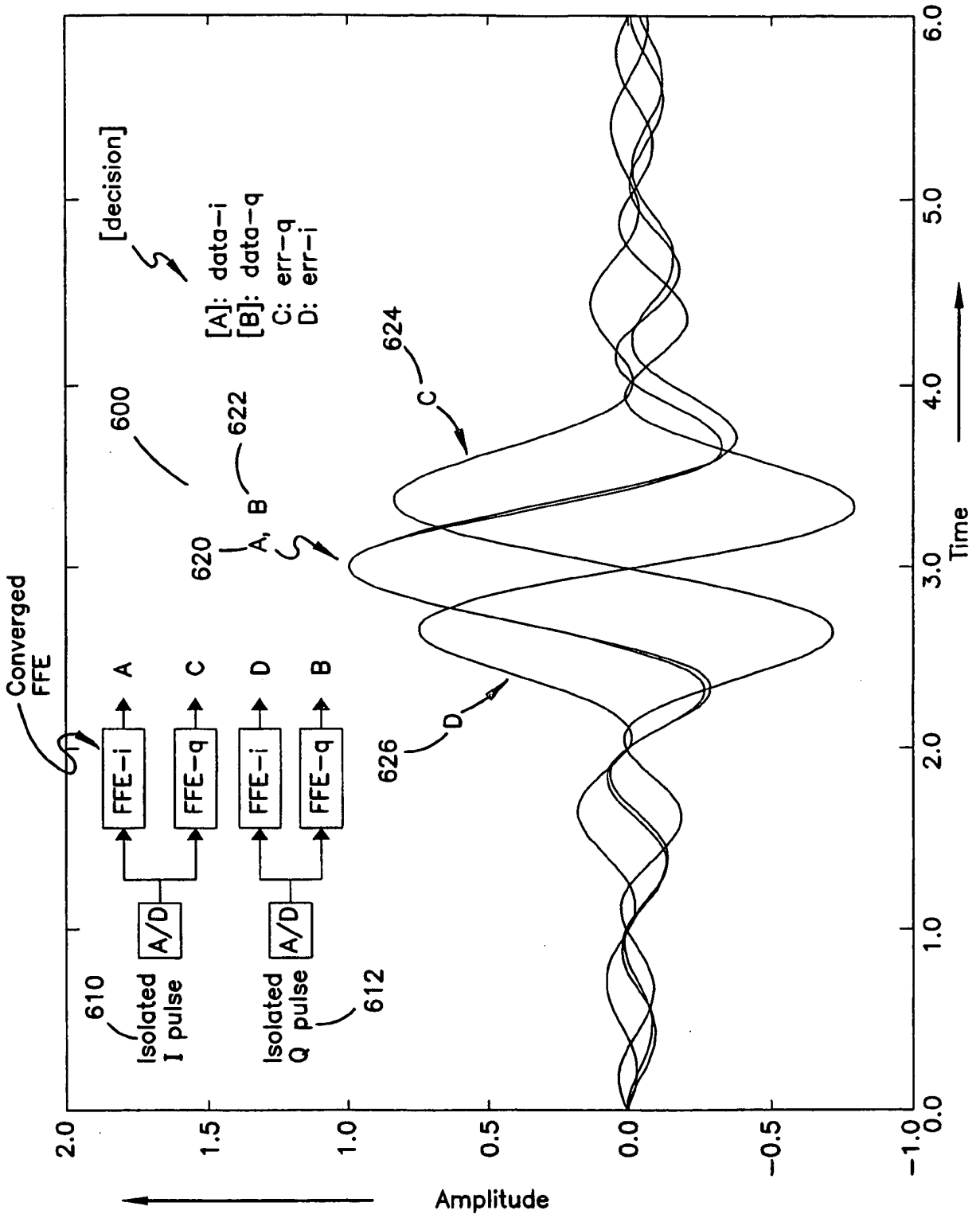
Converged FFE
FFE-i
FFE-q
FFE-i
FFE-q
A
C
D
B
A/D
A/D
610
Isolated I pulse
Isolated Q pulse
612
600
620
622
624
626
A, B
C
D
[decision]
[A]: data-i
[B]: data-q
C: err-q
D: err-i
Amplitude
Time
2.0
1.5
1.0
0.5
0.0
-0.5
-1.0
0.0
1.0
2.0
3.0
4.0
5.0
6.0

FIG. 6

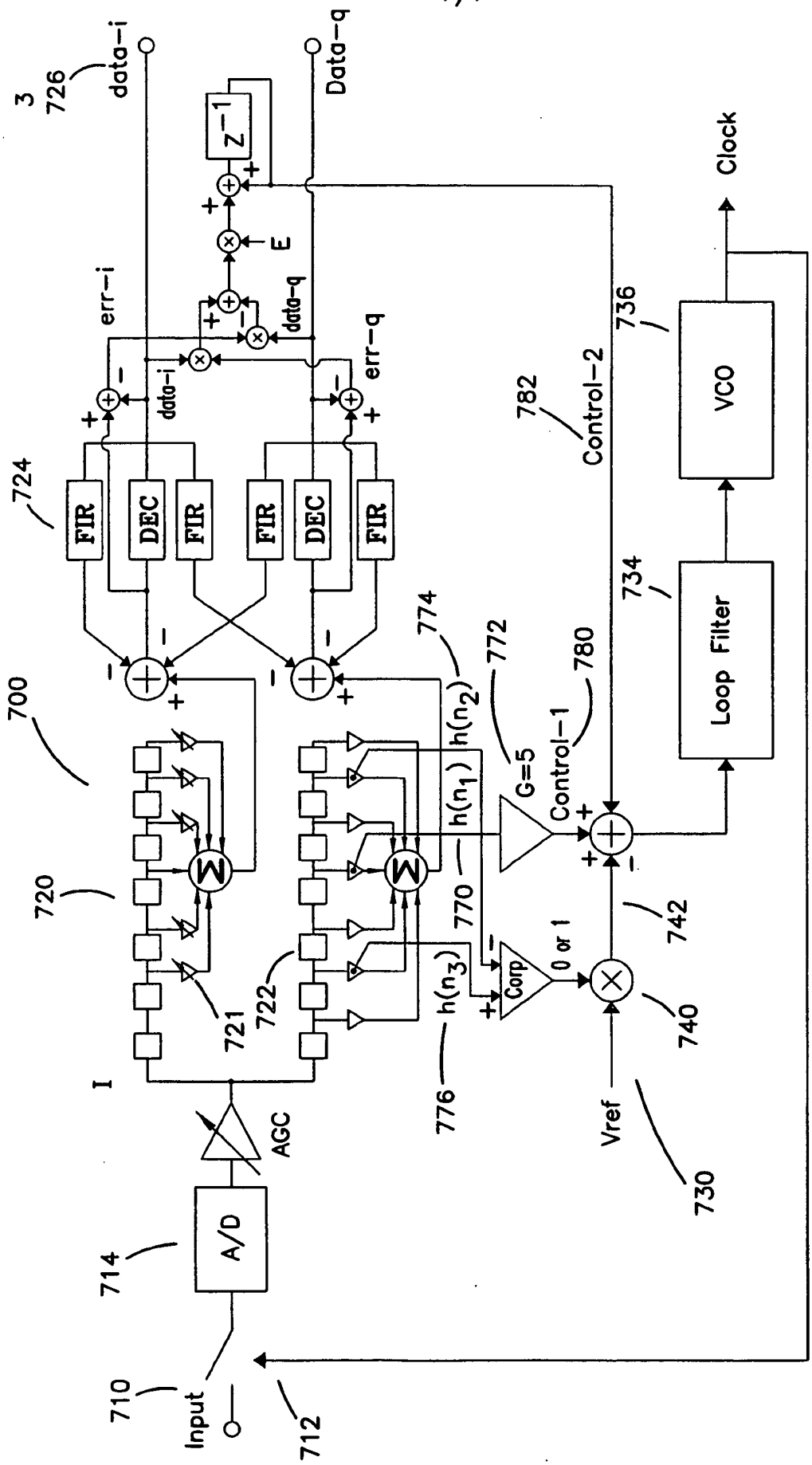
3
726
data-i
Data-q
Z^{-1}
E
err-i
data-q
err-q
data-i
724
FIR
DEC
FIR
FIR
DEC
FIR
782
Control-2
736
VCO
Clock
734
Loop Filter
700
774
772
780
$h(n_2)$
$h(n_1)$
G=5
Control-1
720
770
742
0 or 1
Corp
$h(n_3)$
722
721
740
I
776
Vref
730
AGC
714
A/D
710
Input
712

FIG. 7

INTERNATIONAL SEARCH REPORT

Int. [redacted] al Application No
PCT/US 98/04179

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L7/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 334 313 A (GITLIN RICHARD D ET AL) 8 June 1982 see column 1, line 6 - column 2, line 2 see column 2, line 14 - line 64 see column 4, line 7 - line 17 see column 5, line 27 - line 35	1-4, 11-13, 18-20
A	see column 8, line 13 - column 9, line 31 ---	5-8,15
A	EP 0 368 307 A (NIPPON ELECTRIC CO) 16 May 1990 see column 2, line 1 - line 27 see column 4, line 54 - column 5, line 54 see column 6, line 43 - column 7, line 31 see figures 1,2 --- -/--	1-8, 11-15, 18-20

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publicationdate of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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1

Date of the actual completion of theinternational search	Date of mailing of the international search report
26 May 1998	05/06/1998
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	**Authorized officer** Pieper, T

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	US 5 581 585 A (TAKATORI HIROSHI ET AL) 3 December 1996 see column 2, line 39 - line 44 see column 3, line 54 - column 4, line 23 see column 4, line 56 - column 5, line 35 see column 6, line 17 - line 27 ---	1,2,6, 11-13, 18,19
A	US 4 004 226 A (QURESHI SHAHID U H ET AL) 18 January 1977 see column 3, line 8 - line 68 see figure 4 see column 6, line 6 - line 29 -----	1-4,6, 11,13, 18,19

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 98/04179

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